WHAT IS CLAIMED:

54394

1. A method for transferring vector data in a computer system, the method comprising:

identifying use of vector data in an application program;

implementing at least one vector data instruction for transferring the vector data between a memory and a buffer, the vector data in the buffer being accessible by a processor in the computer system.

2. The method of claim 1 further comprising:

implementing a synchronization instruction to synchronize accessing the vector data with processing the vector data.

3. The method of claim 1 wherein the at least one vector instruction transfers data from the memory to the buffer.

4. The method of claim 1 wherein the at least one vector instruction transfers data from the buffer to the memory.

5. The method of claim 1 wherein the at least one vector instruction transfers data from the buffer to a general purpose register in the processor.

6. The method of claim 1 wherein the at least one vector instruction transfers data from a general purpose register in the processor to the buffer.

7. The method of claim 1 wherein the at least one vector instruction is used to determine whether the buffer is available for use.

8. The method of claim 1 wherein the at least one vector instruction includes information about a vector stream including the starting address of the vector stream.

9. The method of claim 1 wherein the at least one vector instruction includes information about a vector stream including the length of the vector stream.

10. The method of claim 1 wherein the at least one vector instruction includes information about a vector stream including the stride of the vector stream.

11. The method of claim 1 wherein the at least one vector instruction includes information about a vector stream including the starting address of the buffer.

12. The method of claim 1 wherein the at least one vector instruction includes information about a vector stream including the width of the vector data in the data stream.

13. The method of claim 1 wherein the at least one vector instruction includes information about whether the vector data is integer or floating point data.

SUBA5

14. A data processing system comprising:

a data processor;

means for identifying use of vector data in an application program;

at least one vector data instruction for transferring the vector data between a memory and a buffer, the vector data in the buffer being accessible by the data processor; and

a synchronization instruction to synchronize accessing the vector data with processing the vector data.

15. The data processing system of claim 14 wherein the at least one vector instruction transfers data from the memory to the buffer.

16. The data processing system of claim 14 wherein the at least one vector instruction transfers data from the buffer to the memory.

17. The data processing system of claim 14 wherein the at least one vector instruction transfers data from the buffer to a general purpose register in the processor.

18. The data processing system of claim 14 wherein the at least one vector instruction transfers data from a general purpose register in the processor to the buffer.

19. The data processing system of claim 14 wherein the at least one vector instruction is used to determine whether the buffer is available for use.

20. The data processing system of claim 14 wherein the at least one vector instruction includes information about a vector stream including the starting address of the vector stream in the memory.

21. The data processing system of claim 14 wherein the at least one vector instruction includes information about a vector stream including the length of the vector stream.

22. The data processing system of claim 14 wherein the at least one vector instruction includes information about a vector stream including the stride of the vector stream.

23. The data processing system of claim 14 wherein the at least one vector instruction includes information about a vector stream including the starting address in the vector buffer.

24. The data processing system of claim 14 wherein the at least one vector instruction includes information about a vector stream including the width of the vector data in the data stream.

25. The data processing system of claim 14 wherein the at least one vector instruction includes information about whether the vector data is integer or floating point data.

26. The data processing system of claim 14 further comprising:

a vector transfer unit operable to perform burst transfers of the vector data based on the at least one vector instruction.

27. The data processing system of claim 14 wherein the means for identifying use of vector data in an application program is a compiler.

28. The data processing system of claim 27 wherein the compiler identifies use of the vector data based on whether the vector data is used in a program loop.

29. The data processing system of claim 14 wherein the means for identifying use of vector data in an application program includes a vector data indicator, the vector data indicator being recognizable by a compiler as indicating use of the vector data.

30. The data processing system of claim 29 wherein the compiler implements the at least one vector transfer instruction when the compiler recognizes the vector data indicator.

31. A compiler for handling vector data in an application program, comprising:

a source code parser for identifying use of vector data in the application program;

an object code generator operable to implement at least one vector data instruction for transferring the vector data between a memory and a buffer when the source code parser identifies the use of vector data, the object code generator being further operable to implement a synchronization instruction to synchronize accessing the vector data with processing the vector data when the application program is executing.

32. The compiler of claim 31 wherein the at least one vector instruction transfers data from the memory to the buffer.

33. The compiler of claim 31 wherein the at least one vector instruction transfers data from the buffer to the memory.

34. The compiler of claim 31 wherein the at least one vector instruction transfers data from the buffer to a general purpose register.

35. The compiler of claim 31 wherein the at least one vector instruction transfers data from a general purpose register to the buffer.

36. The compiler of claim 31 wherein the at least one vector instruction is used to determine whether the buffer is available for use.

37. The compiler of claim 31 wherein the at least one vector instruction includes information about a vector stream including the starting address of the vector stream, and the length of the vector stream.

38. The compiler of claim 31 wherein the at least one vector instruction includes information about a vector stream including the stride of the vector stream, and the starting address of the buffer.

39. The compiler of claim 31 wherein the at least one vector instruction includes information about a vector stream including the width of the vector data in the data stream.

40. The compiler of claim 31 wherein the at least one vector instruction includes information about whether the vector data is integer or floating point data.

ADD A47